IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:
Application No.:
Filed:
Title:
Commissioner for patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

24504
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339
770-933-9500

ASSIGNEE OF ENTIRE INTEREST
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
8, Li-Hsin Rd. 6
Hsinchu Science Park
Hsinchu, Taiwan 300-77, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 9/2/04

Chien-Wei (Chris) Chou
Director - Intellectual Property Division

Attachment A

No.	Serial No	Filing Date	TSMC No.	Application Title	Assignment (Reel/Frame)
1	10/600,315	06/20/2003	2002-0367	Shared contact for high density memory cell design	014224/0653
2	10/438,646	05/15/2003	2002-0333	Novel embedded dual-port DRAM process	014084/0090
3	10/199,855	07/19/2002	2001-1421	Buildup substrate pad pre-solder bump manufacturing	013131/0272
4	10/644,322	08/20/2003	2002-0428	Characterization methodology for the thin gate oxide device	014418/0900
5	10/167,856	06/11/2002	1999-582/583	Method for making a new metal-insulator-metal (MIM) capacitor structure in copper-CMOS circuits using a pad protect layer	013010/0840
6	10/833,991	04/28/2004	2002-1322	Implementation of protection layer for bond pad protection	Not yet received from the USPTO
7	10/627,013	07/25/2003	2000-0816B	Method with trench source to increase the coupling of source to floating gate split gate flash	recorded 012126/0183 at the parent application USP 6624025
8	10/338,118	01/07/2003	2001-1046	Application of high transmittance attenuating phase shifting mask with dark tone for sub-0.1 micrometer logic device contact hole pattern in 193 lithography	013647/0864
9	10/831,897	04/26/2004	2002-0142	Novel ESD protection scheme for core devices	Not yet received from the USPTO
10	10/358,655	02/05/2003	2001-0994	Novel method of fabricating split gate flash memory cell without select gate-to-drain bridging	013749/0393
11	10/613,607	07/03/2003	2000-0284B	Depletion mode SCR for low capacitance ESD input protection	recorded 012682/0666 at the parent application USP 6610262
12	10/059,835	01/29/2002	2001-1179	Method of wafer edge damage inspection	012573/0695
13	10/082,021	02/21/2002	2000-0084	Novel products derived from embedded flash/EEPROM products	012644/0899
14	10/833,179	04/27/2004	2003-0439	New Architecture to monitor isolation integrity between floating gate and source line	Not yet received from the USPTO
15	10/262,168	10/01/2002	2001-1390	Shallow trench filled with two or more dielectrics for isolation and coupling or for stress control	013355/0903

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16	10/288,197	11/05/2002	1999-0106	Scaled EEPROM cell by metal-insulator-metal (MIM) coupling	013480/0715
17	10/831,868	04/26/2004	2001-0836B	Method for forming an N channel and P channel finfet device on the same semiconductor substrate	recorded 013271/0931 at the parent application 10/235253
18	10/831,848	04/26/2004	2000-0244B	Layout and method to improve mixed-mode resistor performance	recorded 012456/0374 at the parent application USP 6732422
19	10/125,214	04/18/2002	2001-0372	Novel fabrication method for reducing CMOS image sensor noise	012835/0778
20	10/119,335	04/09/2002	2001-0549	Method of forming a capacitor top plate structure to increase capacitance and to improve top plate to bit line overlay margin	012792/0335
21	10/323,981	12/19/2002	2000-0740	Single polysilicon process for DRAM	013617/0788
22	10/056,650	01/28/2002	2003-0387	Multiple mask step and scan aligner	012553/0365

Date: 9/2/04

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